CLAIMS

What is claimed is:

1. A clock recovery adjustment circuit, comprising:

   a) a clock phase adjustment circuit, receiving clock phase information and providing a clock phase adjustment signal;

   b) a clock frequency adjustment circuit, receiving clock frequency information and providing a clock frequency adjustment signal; and

   c) an adder circuit, receiving said clock phase adjustment signal and said clock frequency adjustment signal, and providing a clock recovery adjustment signal.

2. The clock recovery adjustment circuit of Claim 1, wherein said clock frequency adjustment circuit comprises a first multiplier and a first integrator.

3. The clock recovery adjustment circuit of Claim 2, wherein said first multiplier receives said clock frequency information.

4. The clock recovery adjustment circuit of Claim 3, wherein said first multiplier and said first integrator are in series.

5. The clock recovery adjustment circuit of Claim 4, wherein said first integrator provides said clock frequency adjustment signal.

6. The clock recovery adjustment circuit of Claim 1, configured to adjust a clock signal recovered from a data stream.

7. The clock recovery adjustment circuit of Claim 6, wherein said clock frequency information comprises (i) an undershoot determination and (ii) an overshoot determination relative to a bit length of said data stream.

8. The clock recovery adjustment circuit of Claim 6, wherein said clock phase information comprises (i) an early clock phase determination and (ii) a late clock phase determination relative to a data transition of said data stream.

9. The clock recovery adjustment circuit of Claim 6, further comprising logic configured to (i) sample said data stream at predetermined times and (ii) provide said clock frequency information and said clock phase information from sampled data.

10. The clock recovery adjustment circuit of Claim 9, wherein said logic is configured to receive a plurality of predetermined phases of said clock signal.

11. The clock recovery adjustment circuit of Claim 1, wherein said clock phase adjustment circuit comprises parallel first and second clock phase adjustment paths configured to receive said clock phase information, said first clock phase adjustment path comprising a second multiplier and providing a first clock phase adjustment path signal, and said second clock phase adjustment path comprising a third multiplier and a second integrator and providing a second clock phase adjustment path signal.

12. The clock recovery adjustment circuit of Claim 11, wherein said adder circuit comprises a first adder and a second adder.

13. The clock recovery adjustment circuit of Claim 12, wherein said first adder is configured to (i) add said clock frequency adjustment signal and said second clock phase adjustment path signal, and (ii) provide a first adder output.

14. The clock recovery adjustment circuit of Claim 13, wherein said second adder is configured to (i) add said first adder output and said first clock phase adjustment path signal, and (ii) provide said clock recovery adjustment signal.

15. A clock data recovery circuit, comprising:

a) the clock recovery adjustment circuit of Claim 1;

b) a clock recovery circuit, configured to sample a data stream and provide (i) a recovered clock signal and (ii) said clock phase information and said clock frequency information from sampled data.

16. The clock data recovery circuit of Claim 15, wherein said clock recovery circuit comprises a plurality of latches configured to sample said data stream at predetermined times.

17. The clock data recovery circuit of Claim 16, wherein said predetermined times are at regular time intervals corresponding to an integer fraction of said recovered clock signal.

18. The clock data recovery circuit of Claim 17, wherein said integer fraction is $(1/2^n)$, where n is 0 or an integer of at least 1.

19. The clock data recovery circuit of Claim 16, wherein said clock recovery circuit further comprises a plurality of logic gates configured to generate said clock phase information and said clock frequency information from sampled data.

20. The clock data recovery circuit of Claim 15, further comprising a phase locked loop configured to generate a reference clock signal for locking said recovered clock signal.

21. A transceiver, comprising:

a) the clock data recovery circuit of Claim 1;

b) a transmitter communicatively coupled to said clock data recovery circuit, configured to transmit serial data to a network; and

c) a receiver communicatively coupled to said clock data recovery circuit, configured to receive serial data from said network.

22. The transceiver of Claim 21, embodied on a single integrated circuit.

23. The transceiver of Claim 21, further comprising a PLL configured to provide a reference clock signal to said transmitter and said receiver.

24. The transceiver of Claim 21, further comprising a function generator.

25. The transceiver of Claim 24, wherein said function generator comprises a spread spectrum wave generator.

26. The transceiver of Claim 21, further comprising a configuration block configured to store and provide configuration information for said transceiver.

27. A system for transferring data on or across a network, comprising:

a) the transceiver of Claim 21;

b) at least one transmitter port communicatively coupled to said transmitter for transmitting serial data to an external receiver; and

c) at least one receiver port communicatively coupled to said receiver for receiving said data stream.

28. The system of Claim 27, wherein said data stream is a serial data stream.

29. The system of Claim 28, further comprising a converter configured to convert said serial data stream into a parallel data stream.

30. The system of Claim 29, further comprising a storage device configured to receive said parallel data stream.

31. The system of Claim 27, wherein said system is part of a storage network.

32. The system of Claim 27, configured to convert serial data from said network to parallel data for a storage device, and convert parallel data from said storage device to serial data for said network.

33. A network, comprising:

a) a plurality of the systems of Claim 27, communicatively coupled to each other; and

b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to one of said systems.

34. The network of Claim 33, wherein said at least one storage or communications device comprises a storage device.

35. A clock recovery adjustment circuit, comprising:

a) means for adjusting a clock phase from clock phase information;

b) means for adjusting a clock frequency from clock frequency information; and

c) means for providing a clock recovery adjustment signal, coupled to outputs of said means for adjusting said clock phase and said means for adjusting said clock frequency.

36. The clock recovery adjustment circuit of Claim 35, wherein said means for adjusting said clock frequency comprises a first multiplier and a first integrator in series.

37. The clock recovery adjustment circuit of Claim 35, configured to adjust a clock signal recovered from a data stream.

38. The clock recovery adjustment circuit of Claim 37, wherein said clock frequency information comprises (i) an undershoot determination and (ii) an overshoot determination relative to a bit length of said data stream.

39. The clock recovery adjustment circuit of Claim 37, wherein said clock phase information comprises (i) an early clock phase determination and (ii) a late clock phase determination relative to a data transition of said data stream.

40. The clock recovery adjustment circuit of Claim 37, further comprising means for providing said clock frequency information.

41. The clock recovery adjustment circuit of Claim 40, further comprising means for sampling said data stream at predetermined times.

42. The clock recovery adjustment circuit of Claim 41, further comprising means for providing said clock phase information.

43. The clock recovery adjustment circuit of Claim 37, wherein said means for adjusting said clock phase comprises parallel first and second clock phase adjustment paths configured to receive said clock phase information, said first clock phase adjustment path comprising a second multiplier, and said second clock phase adjustment path comprising a third multiplier and a second integrator.

44. The clock recovery adjustment circuit of Claim 37, wherein said means for providing said clock recovery adjustment signal comprises first and second adders.

45. The clock recovery adjustment circuit of Claim 44, wherein said first and second adders are configured to add outputs of said means for adjusting said clock phase and said means for adjusting said clock frequency.

46. A clock data recovery circuit, comprising:

a) the clock recovery adjustment circuit of Claim 37; and

b) means for recovering a clock signal from a data stream, said clock signal having said clock phase and said clock frequency.

47. The clock data recovery circuit of Claim 46, wherein said means for recovering comprises a means for sampling said data stream at predetermined times.

48. The clock data recovery circuit of Claim 47, wherein said means for sampling comprises a plurality of latches.

49. The clock data recovery circuit of Claim 47, wherein said means for recovering comprises means for generating said clock phase information and means for generating said clock frequency information from sampled data.

50. The clock data recovery circuit of Claim 47, further comprising a means for generating a reference clock signal.

51. A transceiver, comprising:

a) the clock data recovery circuit of Claim 47;

b) means for transmitting serial data to a network; and

c) means for receiving a serial data stream from said network.

52. The transceiver of Claim 51, further comprising means for providing a reference clock signal to said means for transmitting and said means for receiving.

53. The transceiver of Claim 51, embodied on a single integrated circuit.

54. A system for transferring data on or across a network, comprising:

a) the transceiver of Claim 51;

b) a first port communicatively coupled to said means for transmitting; and

c) a second port communicatively coupled to said means for receiving.

55. The system of Claim 54, further comprising a means for converting said serial data stream into parallel data.

56. The system of Claim 55, further comprising a means for storing said parallel data.

57. The system of Claim 55, wherein said system is part of a storage network.

58. The system of Claim 56, further comprising a means for converting said parallel data to serial data for said network.

59. A network, comprising:

a) a plurality of the systems of Claim 54, communicatively coupled to each other; and

b) a plurality of means for storing or further communicating data from said serial data stream, each of said means for storing or further communicating being communicatively coupled to one of said systems.

60. A method of adjusting a clock signal recovered from a data stream, comprising the steps of:

a) sampling said data stream at predetermined times;

b) generating clock frequency information and clock phase information from sampled data;

c) altering a frequency and/or a phase of said clock signal in response to said clock frequency information and said clock phase information.

61. The method of Claim 60, wherein said sampling comprises latching said data stream at predetermined intervals.

62. The method of Claim 61, wherein said predetermined intervals are less than two data bit lengths.

63. The method of Claim 62, wherein said predetermined intervals are about one data bit length or less.

64. The method of Claim 60, wherein the step of generating clock frequency information and clock phase information comprises logically comparing data sampled at two or more successive phases of a reference clock.

65. The method of Claim 60, wherein said sampling is performed continuously.

66. The method of Claim 60, wherein said sampling is performed periodically.

67. The method of Claim 60, wherein said sampling is performed conditionally.

68. The method of Claim 60, further comprising repeating said method until said clock signal is phase locked to a reference clock signal.

69. The method of Claim 60, further comprising, after said adjusting step, selecting a reference clock phase to provide to a phase detector receiving the data stream.

70. The method of Claim 60, further comprising adjusting said clock frequency information by a frequency adjustment coefficient.

71. The method of Claim 70, further comprising adjusting said clock phase information by a phase adjustment coefficient and/or a phase-frequency adjustment coefficient.

72. The method of Claim 60, wherein both said frequency and said phase of said clock signal are altered.

73. A method of recovering a clock signal from a data stream, comprising the steps of:

a) receiving said data stream in a phase detector; and

b) performing the method of Claim 60.

74. The method of Claim 73, further comprising providing said clock signal.

75. The method of Claim 73, further comprising providing said data stream from said phase detector.

76. The method of Claim 73, further comprising repeating said performing step until said clock signal is phase locked to a reference clock signal

77. The method of Claim 73, further comprising adjusting a frequency of a second clock signal in response to at least said clock frequency information.

78. The method of Claim 77, further comprising adjusting a phase of said second clock signal in response to at least said clock phase information.